J Mater Sci (2008) 43:3424–3428
DOI 10.1007/s10853-007-2310-6

NANOSMAT 2007 - INTERNATIONAL CONFERENCE ON SURFACES, COATINGS AND NANOSTRUCTURED MATERIALS

Electrical characteristics of Si-nanoparticle/Si-nanowire-based field-effect transistors

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Received: 9 July 2007 / Accepted: 12 November 2007 / Published online: 3 April 2008
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Abstract In this study, Si-nanoparticle(NP)/Si-nanowire-(NW)-based field-effect transistors (FETs) with a top-gate geometry were fabricated and characterized. In these FETs, Si NPs were embedded as localized trap sites in Al_2O_3 top-gate layers coated on Si NW channels. Drain current versus drain voltage ($I_{DS}-V_{DS}$) and drain current versus gate voltage ($I_{DS}-V_{GS}$) were measured for the Si NP/Si NW-based FETs to investigate their electrical and memory characteristics. The Si NW channels were depleted at $V_{GS} = 9$ V, indicating that the devices functioned as *p*-type depletion-mode FETs. The top-gate Si NW-based FETs decorated with Si NPs show counterclockwise hysteresis loops in the $I_{DS}-V_{GS}$ curves, revealing their significant charge storage effect.

Introduction

Recently, nanofloating gate memory (NFGM) devices based on the metal-oxide semiconductor (MOS) structure have attracted considerable attention in the semiconductor industry, due to their potential application in next-generation integrated flash memory. NFGM devices have a structure composed of nanoparticles (NPs) embedded in the oxide layers between the control gate and tunneling layers [1–3]. The NPs can be utilized as localized trap sites in flash memory devices [4]. The use of NPs in NFGM offers lower operating voltages, better endurance characteristics, and faster write/erase speeds, compared with conventional flash memories [5]. In addition, nanowires (NWs) have been investigated in the field of nanoelectronic devices because of their good transport characteristics for charge carriers [6–7]. Especially, Si NWs are more attractive than other semiconducting nanowires, due to their simple synthetic procedure, high crystalline quality, and good electrical characteristics [8–10]. Furthermore, NWs have been used to construct a number of functional devices and device arrays, including field-effect transistors (FETs) [11–14], *p–n* diodes [12–14], bipolar junction transistors [15], and integrated logic circuits [16–18]. These new device functions could open up additional and potentially unexpected opportunities for nanoelectronics systems.

In this study, Si NP/Si NW FETs were fabricated and their electrical characteristics were investigated by conventional current versus voltage ($I-V$) measurements at room temperature. In these FETs, Si NPs were utilized as the localized trap sites, and Si NWs were used as the channels of the charge carriers.

Experiments

The Si NWs were synthesized with low-pressure chemical deposition (LPCVD) [19]. Prior to the synthesis of the Si NWs, a 3-nm-thick Au layer on a silicon substrate was deposited by a thermal evaporator, and the Au-deposited substrate was heated in the chamber filled with argon gas (40 sccm) for 10 min at 500 °C. Au nanodroplets formed on the substrate were used as catalysts for the growth of the Si NWs. 10% diluted SiH_4 in a H_2 gas flowed at a rate of

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40 sccm in a furnace, and a 100-ppm diluted B_2H_6 gas flowed simultaneously at a rate of 5 sccm. Doping concentration was controlled by adjusting the flow rates of SiH_4 and B_2H_6. The flow ratio of silicon to boron was 2000:1 (about 2.498×10^{19} B atoms/cm^3). The Si NWs were grown on the substrate for 15 min at a 45-sccm flow rate of SiH_4/B_2H_6 at 12 Torr at a furnace temperature of 470 °C. The synthesized Si NWs were about 80–110 nm in radius and 20–40 μm in length. High resolution transmission electron microscopy (HRTEM) and scanning electron microscopy (SEM) images of the synthesized Si NWs are shown in Fig. 1a and b, respectively. An energy dispersive X-ray (EDX) spectrum (Fig. 1c) taken from our Si NWs demonstrates that only silicon material is present in the Si NWs; notice that boron material was not detected and that the signals of C and Cu come from the grid. Although the purity of the Si NWs was not determined precisely in this work, the EDX spectrum reveals that the weight percents of any materials except Si in the Si NWs are at least less than 0.1%. Nevertheless, we believe that the Si NWs are very pure. Otherwise, the gate characteristics of the Si NWs would not be observed. The as-grown Si NWs were detached from the SiO_2/Si substrate by sonicating them in methanol solution. The resulting NWs' suspension was dispersed on a *p*-type Si substrate capped with a thermally grown SiO_2 layer of 300-nm thickness. First of all, a 10-nm-thick Al_2O_3 gate dielectric layer was deposited on the channel part by atomic layer deposition (ALD) method [20]. For the growth of the Al_2O_3 dielectric layer, trimethylaluminum (TMA) and high-purity distilled water (H_2O) were used as precursors for the Al_2O_3 deposition. The process temperature and pressure were 150 °C and 200 mTorr, respectively. It should be noted that no Al_2O_3 layer was deposited on the metals under the ALD condition used in this work. A poly-Si thin film with a thickness of 5 nm was then deposited on the substrate using LPCVD process. To form Si NPs, the as-deposited poly-Si thin film was etched by a solution of NHO_3, H_2O, and HF in a weight 50:20:1 ratio. Cross-sectional HRTEM and SEM images of the Si NPs present on the p-Si NW are shown in Fig. 2a and b, respectively. The HRTEM image demonstrates that the diameter of the p-Si NW is about 100 nm and that the Si NW is covered with a 10-nm-thick Al_2O_3 layer. These HRTEM and SEM images also reveal that well-defined Si NPs with spherical shape are separated from each other and uniformly distributed on the Si NW coated with the Al_2O_3 layer. The average diameter of the NPs was 5 nm. Positive photoresist (PR) was spin-coated

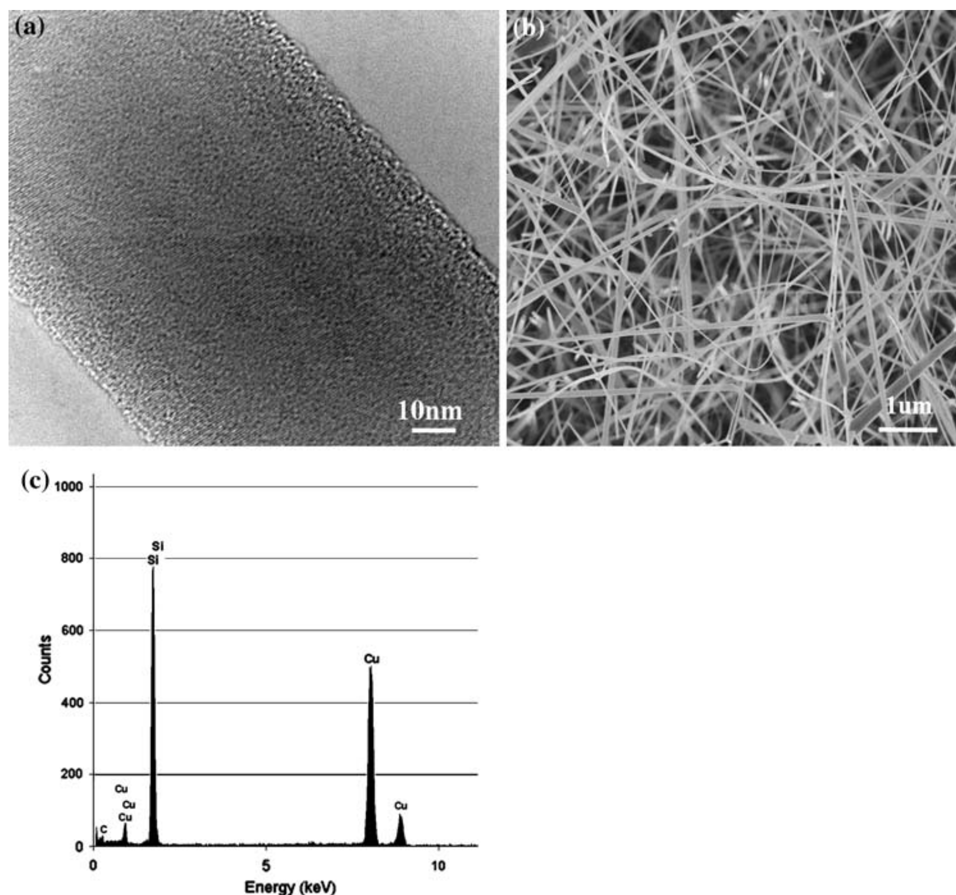

Fig. 1 (**a**) The HRTEM image of a selected Si NW, (**b**) the SEM image of the synthesized Si NWs, and (**c**) the EDX spectrum taken from the Si NWs

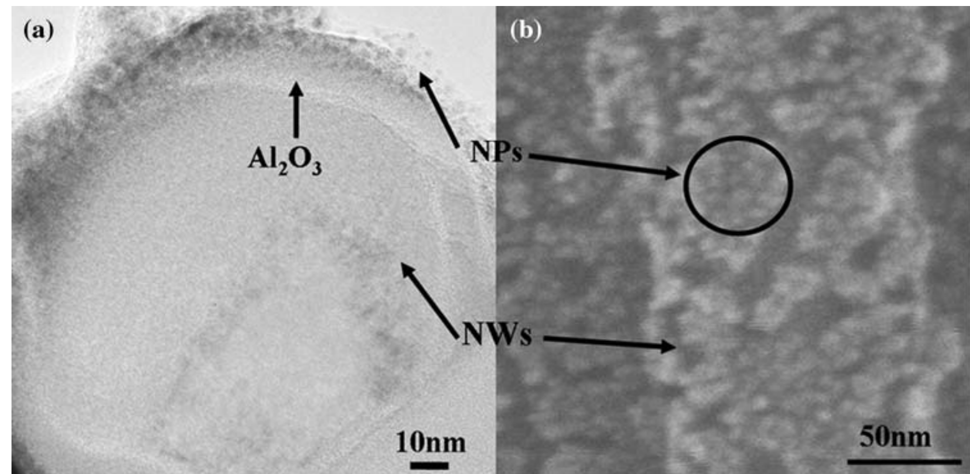

Fig. 2 (**a**) The cross-sectional HRTEM image of the Si NP-NW structure and (**b**) the SEM image of the Si NP-NW structure

on the nanostructures on the top of the substrate, and source and drain regions were patterned at the ends of a selected single Si NW via a conventional photolithography process. For contacting the NW with source and drain metal electrodes, some parts of the Al_2O_3 layer present on the ends of the Si NW were etched out using H_3PO_4, and residual PR was washed out by acetone and distilled water. The source and drain metal electrodes were formed by the thermal evaporation of Ti (50 nm) and Au (50 nm). The control oxide layer composed of a 25-nm-thick Al_2O_3 layer was deposited on the whole structure by the ALD method. To form a top-gate electrode, Ti (50 nm) and Au (50 nm) metals were formed on a central part of the Si NW cladded with the Si NPs and the Al_2O_3 layer after patterning of the 3-μm-long gate region and by the subsequent lift-off process. The schematic structure and SEM image of the fabricated NP-NW FET are shown in Fig. 3a and b, respectively. For our FET structure, the channel length between the source and the drain electrode is 6 μm, the gate length is 3 μm, the thickness of the control oxide layer is 25 nm, and the thickness of the tunneling oxide layer is 10 nm. In this structure, Si NPs were embedded in the Al_2O_3 layer as the localized trap sites. For comparison, the dimensions of a device demonstrated by the Lieber group are given as follows [21]. In the device, the channel length of the top-gate device was 2 μm, the thickness of the control oxide layer was 30 nm, and the thickness of the tunneling oxide layer was 9 nm. The two oxide layers were HfO_2 (k=25) ones deposited by an ALD method.

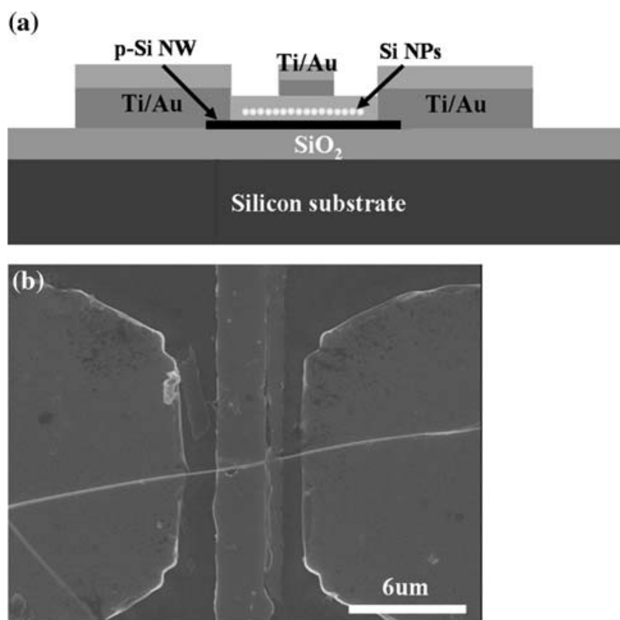

Fig. 3 (**a**) The cross-sectional schematic of the Si NP-NW FET and (**b**) the SEM image of the Si NP-NW FET

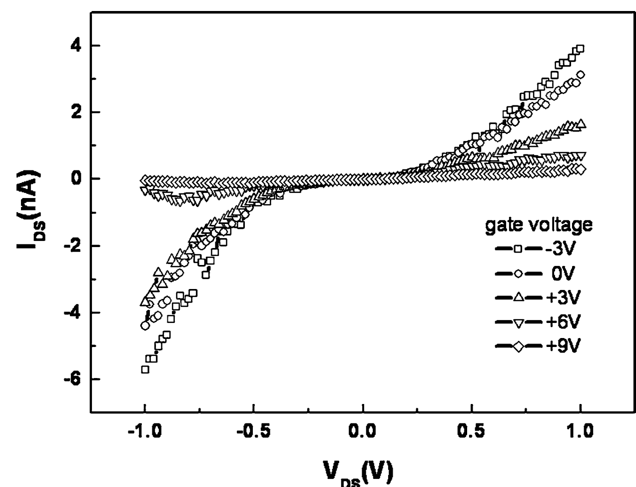

Fig. 4 $I_{DS}-V_{DS}$ characteristics of the Si NP-NW FET at various gate voltages (V_g)

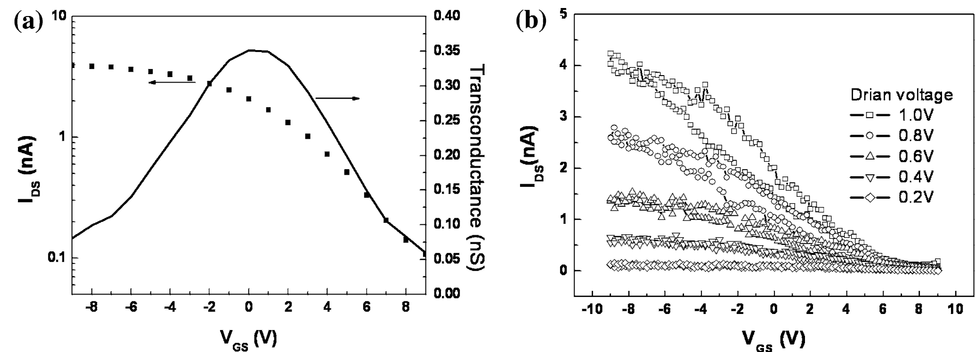

Fig. 5 (**a**) $I_{DS}-V_{GS}$ transfer and transconductance curves at V_{DS} = 1 V and (**b**) the $I_{DS}-V_{GS}$ characteristics with double sweeping at various V_{DS}

Result and discussion

The electrical characteristics of a representative Si NPs/Si NW FET are shown in Fig. 4. The family of drain current versus drain voltage ($I_{DS}-V_{DS}$) curves shows that the I_{DS} increases with increasing V_{DS}. Its characteristics exhibit Schottky contact behavior. The shape of $I_{DS}-V_{DS}$ curve shows that there still exists an energy barrier which interrupts the flowing of the charge carriers. The slope of the $I_{DS}-V_{DS}$ curve decreases as the gate voltage, V_{GS}, varies from −3 to 9 V. The decreasing slope demonstrates that the Si NW is *p*-type. The $I_{DS}-V_{GS}$ transfer and transconductance curves taken at V_{DS} = 1 V are plotted in Fig. 5a. In the $I_{DS}-V_{DS}$ transfer curve, the I_{on}/I_{off} ratio is close to about 10^2. The transconductance curve reveals that the peak transconductance, g_m, is 351 pS at V_{GS}= 0 V and that the threshold voltage is 7.8 V. In addition, the capacitance of the gate dielectrics and the field-effect mobility of the charge carriers may be calculated as follows. The capacitance, *C*, of the hybrid NP-NW device is found to be 5.05 fF from the formula [21], $C = 2\pi\varepsilon_r\varepsilon_0 L_g/\ln(r_g/r_{NW})$, where ε_r is the dielectric constant of Al_2O_3 (8.4), L_g is the gate length (3 μm), r_g is the radius of the Al_2O_3-coated NW (160 nm), and r_{nw} is the radius of the NW (100 nm). The field-effect mobility, μ_{FE}, is estimated to be 1.8 cm^2/Vs at V_{DS} = 1 V on the basis of the formula [22], $\mu_{FE} = L_c L_g g_m r_g / C V_{DS} r_{NW}$, where L_c is the channel length (6 μm). To investigate the memory characteristics, the family of $I_{DS}-V_{GS}$ curves for double sweeping of the drain voltage was obtained from the Si NP/Si NW-based FET (Fig. 5 b). Its $I_{DS}-V_{GS}$ characteristics examined in each different drain voltage were biased from the negative to positive voltage and then from the positive to negative voltage. The top-gate Si NW-based FET decorated with Si NPs shows counterclockwise hysteresis loops in the $I_{DS}-V_{GS}$ curves, indicating the significant charge storage effect. The observation indicates that holes in the Si-NW channel can be injected to the localized trap sites of the Si NPs and that the holes can be extracted from the NPs reversely.

Conclusion

In this study, Si NP/Si NW-based FETs with top-gate geometry were fabricated. In the FETs, Si NPs were embedded in Al_2O_3 top-gate layers as localized trap sites. $I_{DS}-V_{DS}$ and $I_{DS}-V_{GS}$ were measured for the Si NP/Si NW-based FETs to investigate their electrical and memory characteristics. The family of $I_{DS}-V_{GS}$ curves for the double sweeping of the drain voltage obtained from the Si NP/Si NW-based FETs revealed counterclockwise hysteresis loops. The observation indicates that holes in the Si NW channel can be injected to the localized trap sites of the Si NPs and that the holes can be extracted from the NPs reversely.

Acknowledgement This work was supported by the Center for Integrated-Nano-Systems (CINS) of the Korea Research Foundation (KRF-2006-005-J03601), the Korea Science and Engineering Foundation (KOSEF) through the National Research Lab. Program (R0A-2005-000-10045-02 (2007)), the Nano R&D Program (M10703000980-07M0300-98010), and "SystemIC2010" project of Korea Ministry of Commerce, Industry and Energy.

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